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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/410,642
Filing Date: October 01, 1999
Appellant(s): EDWARDS ET AL.

Stuart T. Langley, Reg. No. 33,940
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For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed June 2, 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences, which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal

is contained in the brief. However, the statement fails to mention the related co-pending Application No. 09/410,646.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The Examiner acknowledges the Appellant's statement that the rejection of claims 1-19 and 21-36 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

4,486,826	Wolff et al.	12-1984
6,032,271	Goodrum et al.	2-2000
6,055,596	Cepulis	4-2000
4,918,693	Ardini, Jr. et al.	4-1990

5,652,754	Pizzica	7-1997
5,678,028	Bershteyn et al.	10-1997
4,942,552	Merrill et al.	7-1990

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-6, 11-13, 15-18, 21, 22, and 25-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Wolff et al., U.S. Patent 4,486,826.

Referring to claims 1, 22, 33, and 34:

a. In column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an address (packet routing information).

b. In column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an identical set of cycle definition, address, data, parity and other signals that can be compared to warn of erroneous information transfer between units (packets of information, wherein each packet comprises a number of fields containing information).

c. In column 14, lines 7-8, Wolff et al. disclose that each data transfer cycle has at least four such timing phases. Further, in column 14, lines 28-68 continued in column 15, lines 1-45, Wolff et al. disclose a definition phase containing address information and a response phase containing data. By definition a packet is a group of bits that perform a function. In Wolff et al. a cycle is a group of bits with different phases that perform a single function. Therefore, Wolff et al. teach a packet containing information including both data

and packet routing information. Further, in column 14, lines 45-58, Wolff et al. teach that each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data.

d. In column 2, lines 31-35, Wolff et al. disclose a computer system (a functional circuit), which has a processor module with a processing unit, a random access memory unit, and peripheral control units (plurality of modules), and it has a single bus structure which provides all information transfers between the several units of the module (interconnect for information transfer).

e. In column 2, lines 31-35, Wolff et al. disclose that the computer system has a single bus structure, which provides all information transfers between the several units of the module (circuitry for receiving at least part of said information).

f. In column 2, lines 48-56, Wolff et al. disclose that the computer system provides fault detection at the level of each functional unit within a processor module. To attain this feature, error detectors monitor hardware operations within each unit and check information transfers between the units (circuitry for determining if said at least part of said information satisfies one or more conditions).

g. In column 2, lines 48-56, Wolff et al. disclose that the detection of an error causes the processor module to isolate the bus or unit which caused the error from transferring information to other units (circuitry for performing one or more

actions in response to the determination that at least part of the information satisfies one or more conditions).

Referring to claim 2, in column 11, lines 36-54, Wolff et al. disclose that in response to the fault signal, the control section produces an error signal (trace message) that the X bus transmits to all units of the module.

Referring to claims 3 and 4, in column 11, lines 50-54, Wolff et al. disclose that any failing unit also produces an interrupt signal that causes the central processing unit of the module (one or more CPUs) to interrogate the different units to locate the faulty one.

Referring to claim 5, in column 2, lines 48-56, Wolff et al. disclose that the detection of an error causes the processor module to isolate the bus or unit which caused the error from transferring information to other units (prevent one or more modules from being granted access to the interconnect).

Referring to claims 6 and 11, in column 40, lines 63-68 continued in column 41, lines 1-2, Wolff et al. disclose a broken flip-flop to disable the drivers of a peripheral device in response to a fault.

Referring to claim 12, in column 40, lines 56-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator that compares peripheral (module) output signals (information on interconnect) with corresponding output signals from the check control section (match conditions). In response to an invalid comparison, the comparator switches a so-called broken flip-flop to disable the drivers (determining circuitry using a comparator).

Referring to claims 13 and 15, in column 25, lines 32-40, Wolff et al. disclose that the central processing unit (circuit) has two subsystems and control circuits within the unit that take the unit off-line upon detection of an error (precondition: enabled or not enabled). Further, in column 40, lines 56-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator that compares peripheral (module) output signals (information on interconnect) with corresponding output signals from the check control section (match conditions). In response to an invalid comparison, the comparator switches a so-called broken flip-flop to disable the drivers (determining circuitry using a comparator).

Referring to claims 16 and 17, in figures 5A, 5B, and 1, and in column 28, lines 21-35, Wolff et al. disclose latch 120 which is between the interconnect and the processor module (circuitry external to said circuit). The latch provides temporary storage of output data so that in the event any error is reported on the buses, the operating sequence in which the error was reported can be duplicated and the data retransmitted on the A bus 42 (external circuitry is enabled).

Referring to claims 18 and 21, in column 3, lines 57-68, Wolff et al. disclose that the bus carries cycle-definition (type of transaction to which the information relates), address (address of the information), data, parity, and other signals that can be compared to warn of erroneous information transfer between units (match conditions). The information comprising packets of information, requests, and response is inherent to the information mentioned above that is sent over a bus.

Referring to claim 25, in column 20, lines 35-55, Wolff et al. disclose an arbitration network (arbiter) which provides an automatic hardware determination of which unit, or pair of partner units, that requests access to the bus structure (interconnect) has priority to initiate an operating cycle (granted access).

Referring to claim 26, in column 20, lines 35-55, Wolff et al. disclose that the processor module (determining circuitry) has two arbitration networks (arbiter) connected to bus A and bus B.

Referring to claims 27 and 31, in column 3, lines 34-47, Wolff et al. disclose that upon detection of an error-manifesting fault in any unit, that unit is isolated and placed off-line so that it cannot transfer information to other units of the module. The partner of the off-line unit continues operating and thereby enables the entire module to continue operating, normally with essentially no interruption.

Referring to claim 28, in the abstract, Wolff et al. disclose a bus.

Referring to claims 29, 30, and 32, in column 2, lines 48-63, Wolff et al. disclose error detectors (debug module) at the level of each functional unit (module). Further, in column 40, lines 63-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator, which switches a so-called broken flip-flop to disable the drivers upon detection of an error (circuitry for performing at least one action). The comparator is part of the control unit, which is part of the functional unit (circuitry in said debug module).

Claims 1, 22, 33, 34, 35 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Goodrum et al., U.S. Patent 6,032,271.

Referring to claims 1, 22, 33, 34, 35, and 36:

a. In the Abstract, Goodrum et al. disclose a bus with devices connected to it (an interconnect and a plurality of modules connected to said interconnect for putting packets of information onto the interconnect).

b. In Figure 15A and the table in column 14, Goodrum et al. disclose that each packet comprises a number of fields containing information including both data and packet routing information, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data).

c. In column 45, lines 16-40, Goodrum et al. disclose that when a transaction on the PCI bus does target the QPIF, the slave state machine enters a SLAVE_DAC dual address cycle state if the p2q_ dac_flag is asserted and an address parity error has not occurred (p2q_perr_is low). If the transaction is not a dual address cycle and is a posted memory write request, and if a parity error has not occurred in the address phase, the slave state machine loads the write counters (i.e., asserts load_write_counter) and determines whether it can accept the transaction (circuitry for receiving at least part of said information; circuitry for determining if said at least part of said information satisfies one or more conditions; and circuitry for performing one or more actions in response to the determination that at least part of the information satisfies one or more conditions).

d. Fields containing information, including a routing field, and address field, a source field, a transaction type field, a transaction identifier field, and an operation code field are inherent to the PCI bus of Goodrum et al.

Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S Patent 4,486,826 as applied to claim 6 above, and further in view of Cepulis, U.S. Patent 6,055,596.

Referring to claim 7, in column 40, lines 63-68 continued in column 41, lines 1-2, Wolff et al. disclose a so-called broken flip-flop to disable the drivers of a peripheral device (module) in order to prevent it from putting further information onto the bus (interconnect). However, Wolff et al. don't explicitly disclose using a register for preventing a module from putting information onto the interconnect. In column 75, lines 3-10, Cepulis discloses that the CPU can power up one of the slots by writing a "1" to a corresponding bit of a slot enable register and disable the slot by writing a "0" to this bit. It would have been obvious to one of ordinary skill at the time of the invention to include the slot enable register of Cepulis into the system of Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification because as disclosed by Wolff et al. a switching means is needed to disconnect a peripheral device. The slot enable register of Cepulis is one type of switching means used to disconnect a peripheral device.

Referring to claim 8, in column 75, lines 3-10, Cepulis discloses that the CPU can power up one of the slots by writing a "1" to a corresponding bit of a slot enable register and disable the slot by writing a "0" to this bit (the register comprises one bit for each

module and the value of said bit determines if the respective module is prevented from putting further information into the interconnect).

Referring to claim 9, in column 75, lines 3-10, Cepulis discloses that the CPU (one module arranged to access the register non-intrusively) can power up one of the slots by writing a "1" to a corresponding bit of a slot enable register and disable the slot by writing a "0" to this bit.

Referring to claim 10, in column 75, lines 3-10, Cepulis discloses a slot enable register with a corresponding bit for each slot (the location being independent of the address of the module).

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826 as applied to claim 13 above, and further in view of Ardini, Jr. et al., U.S. Patent 4,918,693. In column 40, lines 56-68 continued in column 41, lines 1-2, Wolff et al. disclose a comparator that compares peripheral (module) output signals (information on interconnect) with corresponding output signals from the check control section (match conditions). In response to an invalid comparison, the comparator switches a so-called broken flip-flop to disable the drivers (determining circuitry using a comparator). However, Wolff et al. don't explicitly disclose satisfying a precondition by having match conditions occurring a predetermined number of times. In column 8, lines 9-14, Ardini, Jr. et al. disclose a diagnostic program that, after a certain number of parity error signals are received from board 202, it will send a code to disable the parity check circuit output. It would have been obvious to one of ordinary skill at the time of the invention to include the parity error signal threshold of Ardini, Jr. et al. into the system of

Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification because a parity check circuit can become faulty so that it continuously generates a parity error signal on its output (see Ardini, Jr. et al.: column 8, lines 7-9). In this case, to check for a faulty parity circuit would require a precondition.

Claims 19 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826 as applied to claim 1 above, and further in view of Pizzica, U.S. Patent 5,652,754.

Referring to claims 19 and 35, in column 2, lines 48-56, Wolff et al. disclose that the computer system provides fault detection at the level of each functional unit within a processor module. To attain this feature, error detectors monitor hardware operations within each unit and check information transfers between the units (circuitry for determining if said at least part of said information satisfies one or more conditions). Further, in column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an identical set of cycle definition, address, data, parity and other signals that can be compared to warn of erroneous information transfer between units (packets of information). However, Wolff et al. don't explicitly disclose storing circuitry to store the information which satisfies the at least one condition. In column 2, lines 53-60, Pizzica discloses a signature storage device that stores a fault free signature from a functional digital module and faulty signatures obtained by shorting and opening each of the circuit nodes thereof. It would have been obvious to one of ordinary skill at the time of the invention to include the faulty signature storing of Pizzica into the system of Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification

because *the recorded signatures can be used for subsequent pass/fail determination of digital modules that are tested* (see Pizzica: column 1, lines 46-48).

Further, referring to claim 35:

a. In column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an address (packet routing information).

b. In column 14, lines 7-8, Wolff et al. disclose that each data transfer cycle has at least four such timing phases. Further, in column 14, lines 28-68 continued in column 15, lines 1-45, Wolff et al. disclose a definition phase containing address information and a response phase containing data. By definition a packet is a group of bits that perform a function. In Wolff et al. a cycle is a group of bits with different phases that perform a single function. Therefore, Wolff et al. teach a packet containing information including both data and packet routing information. Further, in column 14, lines 45-58, Wolff et al. teach that each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data.

c. In column 2, lines 31-35, Wolff et al. disclose a computer system, which has a processor module with a processing unit, a random access memory unit, and peripheral control units (plurality of modules), and it has a single bus structure which provides all information transfers between the several units of the module (interconnect for information transfer).

d. In column 2, lines 31-35, Wolff et al. disclose that the computer system has a single bus structure, which provides all information transfers between the several units of the module (circuitry for receiving at least part of said information).

e. In column 2, lines 48-56, Wolff et al. disclose that the computer system provides fault detection at the level of each functional unit within a processor module. To attain this feature, error detectors monitor hardware operations within each unit and check information transfers between the units (circuitry for determining if said at least part of said information satisfies one or more conditions).

Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826 as applied to claim 22 above, and further in view of Bershteyn et al., U.S. Patent 5,678,028.

Referring to claim 23, in the abstract, Wolff et al. disclose a fault-tolerant computer system comprising a processor unit, a memory unit, one or more peripheral control units, and a bus structure. However, Wolff et al. don't explicitly disclose that these circuits are an integrated circuit. In the Background of Bershteyn et al., a system-on-a-chip debugger is disclosed. It would have been obvious to one of ordinary skill at the time of the invention to make the system of Wolff et al. into the system-on-a-chip debugger of Bershteyn et al. into the. A person of ordinary skill in the art would have been motivated to make the modification because an entire system can be fabricated on

a single wafer decreasing the cost of the entire system (see Bershteyn et al.: column 1, lines 45-67).

Referring to claim 24, in the abstract Wolff et al. disclose a computing module (external module), one or more peripheral control units (modules), and a bus structure (interconnect).

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wolff et al., U.S. Patent 4,486,826, and further in view of Merrill et al., U.S. Patent 4,942,552.

Referring to claim 36:

a. In column 3, lines 61-64, Wolff et al. disclose that the A and B buses each carry an identical set of cycle-definition, address, data, and parity signals. However, Wolff et al. don't explicitly disclose having fields/signals that contain information including a source field, a transaction type field, a transaction identifier field, and an operation code field. In column 7, lines 26-30, Merrill et al. disclose that both the read commands and the write commands contain parameters which specify the data to be moved, including the source address, destination address, and the length of data to be moved. In column 19, lines 42-50, Merrill et al. disclose an ID field that contains an operation code which identifies one command message from said predetermined set of command messages. In column 23, lines 22-25, Merrill et al. disclose remote command messages including at least first and second remote command message types. In column 11, lines 18-21, Merrill et al. disclose a transaction number that is included in both the output message and the reply to match up the commands

and responses. It would have been obvious to one of ordinary skill at the time of the invention to include the fields of Merrill et al. into the system of Wolff et al. A person of ordinary skill in the art would have been motivated to make the modification because these fields can be used to in comparison to other signals so as to warn of erroneous information transfer between units (see Wolff et al.: column 3, lines 63-64).

b. In column 2, lines 31-35, Wolff et al. disclose a computer system (a functional circuit), which has a processor module with a processing unit, a random access memory unit, and peripheral control units (plurality of modules), and it has a single bus structure which provides all information transfers between the several units of the module (interconnect for information transfer that is not a circuit-switched bus).

c. In column 14, lines 7-8, Wolff et al. disclose that each data transfer cycle has at least four such timing phases. Further, in column 14, lines 28-68 continued in column 15, lines 1-45, Wolff et al. disclose a definition phase containing address information and a response phase containing data. By definition a packet is a group of bits that perform a function. In Wolff et al. a cycle is a group of bits with different phases that perform a single function. Therefore, Wolff et al. teach a packet containing information including both data and packet routing information. Further, in column 14, lines 45-58, Wolff et al. teach that each module has a unique identification on the interconnect and

wherein the routing information identifies at least one of the modules associated with the data.

d. In column 2, lines 31-35, Wolff et al. disclose that the computer system has a single bus structure, which provides all information transfers between the several units of the module (circuitry for receiving at least part of said information).

e. In column 2, lines 48-56, Wolff et al. disclose that the computer system provides fault detection at the level of each functional unit within a processor module. To attain this feature, error detectors monitor hardware operations within each unit and check information transfers between the units (circuitry for determining if said at least part of said information satisfies one or more conditions).

f. In column 2, lines 48-56, Wolff et al. disclose that the detection of an error causes the processor module to isolate the bus or unit which caused the error from transferring information to other units (circuitry for performing one or more actions in response to the determination that at least part of the information satisfies one or more conditions).

(11) Response to Argument

With respect to the argument: **A. Whether claims 1-6, 11-13, 15-18, 21, 22, and 25-34 are anticipated by Wolff et al.**, on page 4, the Applicant argues, "The 'set of signals' is a square peg which the Examiner attempts to force into the round holes defined by the packets of information and information-containing packets of claims 1,

22, 33, and 34. To do this, the Examiner chooses to construe the definition of a packet as 'a serial stream of clocked data bits'. There is no authority cited for this definition, and this definition contradicts the commonly accepted meaning of the word 'packet' as set out in various authoritative definitions of record." The Examiner respectfully disagrees. On page 787, under the definition of packet, specifically no. (7), the IEEE 100, The Authoritative Dictionary of IEEE Standards and Terms defines a packet as being a serial stream of clocked data bits. The Examiner would like to note that this definition can be considered to be a commonly accepted meaning of the word "packet" and that this definition is amongst 14 definitions given for the word "packet". Also, on pages 4-5, the Applicant provides a definition of a packet taken from Newton's Telecom Dictionary, 18th Edition (2002). The Examiner would like to note that the Applicant's invention disclosed in the specification does not involve a telecom system and thus makes this definition irrelevant. The Examiner realizes that both the Examiner and the Applicant could easily cite definitions back and forth, however, for purposes of argument the Examiner will address the Applicant's definition of a packet and show how Wolff et al. teach this definition.

With respect to the argument: **A. Whether claims 1-6, 11-13, 15-18, 21, 22, and 25-34 are anticipated by Wolff et al.**, on page 5, the Applicant argues, "Packet routing information, described generally at page 5 of the specification, is a particular type of information that does not appear in a bus-type interconnect of the Wolff reference. The set of signals in Wolff et al. is not routed—it is coupled end-to-end by the physical interconnect. The set of signals in Wolff et al. do not contain routing information as

there is but one source and one destination possible. The set of signals in Wolff et al. is not a unit of data, it is a collection of separate signals. Accordingly, Wolff et al. do not show a packet as called for in claims 1 and 22." The Examiner respectfully disagrees. In column 3, lines 57-68, Wolff et al. disclose that the A and B buses each carry an identical set of cycle definition, address (packet routing information), data, parity, and other signals. Further, in Figure 1 and in column 10, lines 4-7, Wolff et al. disclose that each unit 12 through 28 is connected to all the buses of the bus structure including the A and B buses (reference nos. 42 and 44). Therefore, there is more than one source and one destination possible in the system of Wolff et al., hence the necessity for an address or packet routing information. This is further shown in column 14, lines 49-51, where Wolff et al. disclose that the bus master unit asserts the physical address signals identifying the memory or **I/O location** for the cycle.

With respect to the argument: **A. Whether claims 1-6, 11-13, 15-18, 21, 22, and 25-34 are anticipated by Wolff et al.**, on page 6, the Applicant argues a definition taken from Newton's Telecom Dictionary for an information packet. The Examiner would like to note that this definition is not relevant to the Applicant's invention since the Applicant's invention concerns a bus on an integrated circuit and not a telecom system. Further, the Applicant argues, "In Wolff et al. the size of the set of information is determined by the number of signal lines (called 'sets of conductors in col. 3, line 60) in the bus, and not by a protocol used. In contrast, the claims call for packets of information in the ordinary meaning of that term where the packet size is determined by a protocol choice, not a hardware limitation." The Examiner respectfully disagrees.

There is no mention whatsoever of a size of the information or a protocol in any of the claims. Still further, the Applicant argues that the Wolff et al. reference contains circuit switched type connections. However, this is incorrect since a circuit switched connection requires an individual interconnect for each component. An example would be an old telephone switchboard where one customer would speak to another via a single separate telephone line. This is not the case in Wolff et al. since Wolff et al. discloses amongst other things addresses used for routing information and more importantly a group of devices connected to a single bus.

With respect to the argument: **A. Whether claims 1-6, 11-13, 15-18, 21, 22, and 25-34 are anticipated by Wolff et al.**, on page 6, the Applicant argues, "Further, claims 1, 22, 33, and 34 call for a determination of whether the information in a packet satisfies one or more (emphasis by Applicant) conditions. Because Wolff et al. compare a binary signal to another binary signal there is one and only one 'condition' that can be satisfied. Specifically, Wolff et al. can only determine if the signals match, and determine if any other condition is satisfied." The Examiner respectfully disagrees. The Examiner would like to point out that this limitation is written in the alternative; therefore only one condition has to be satisfied. By Applicant's own admission, the reference of Wolff et al. teach that one condition is satisfied.

In conclusion the Examiner would like to note in column 3, lines 57-68, Wolff et al. disclose that the A and B buses each carry an identical set of cycle definition, address (packet routing information), data (the data), parity, and other signals. Further, a transfer cycle as defined by Wolff et al. would be a packet. A cycle is four phases and

is done over many clock cycles (see Wolff et al.: column 13, line 63 through column 14, line 20). It is well known that a packet, when it is processed, is broken into chunks of bits that are processed on different clock cycles. Each phase in the cycle can be considered a chunk of bits. Since there is a phase containing the routing information and a phase containing data, all of which contained in a single cycle, then Wolff et al. teach a packet containing information including both data and packet routing information sent as a unit as defined by the Applicant.

With respect to the argument: **B. Whether claims 1, 22, and 33-36 are anticipated by Goodrum et al.**, on pages 6-7, the Applicant argues, "Like the Wolff et al. reference discussed above, Goodrum et al. do not show or suggest monitoring information from packets containing information (or information-containing packets). Goodrum et al. describe several bus types including PCI, EISA, and local bus. None of these are described as packet bus architectures or as conveying packets. It is quite telling that in 185 pages of text and drawings, Goodrum does not once use the word "packet". Nevertheless, the Office Action states that 'In the Abstract, Goodrum et al. disclose...an interconnect and a plurality of modules connected to said interconnect for putting packets of information onto the interconnect...' The Abstract contains no such language, and the Office Action simply uses Appellant's claim as a template for abstracting the word 'bus' into a rejection." The Examiner respectfully disagrees. The Applicant has chosen to scan the document for the word "packet" rather than consider the definition of a packet and then read the entire document with respect to the definition. This is evident in the fact that the Applicant has chosen to ignore the

Examiner's rejection in which it is pointed out where in the reference a packet is disclosed, specifically in a table in column 14 and in Figure 15A. The Final Office Action specifically states that in Figure 15A and the table in column 14, Goodrum et al. disclose that each packet comprises a number of fields containing information including both data and packet routing information, wherein each module has a unique identification on the interconnect and wherein the routing information identifies at least one of the modules associated with the data. Further, the Examiner cites the Abstract as containing a bus with devices connected to it in order to address the limitation of: an interconnect and a plurality of modules connected to said interconnect. It is disclosed that these devices are putting packets on the interconnect throughout the reference of Goodrum et al. since the data being used on the interconnect is shown in column 14.

With respect to the argument: **B. Whether claims 1, 22, and 33-36 are anticipated by Goodrum et al.**, on page 7, the Applicant argues, "Further, the Examiner points to Goodrums' Fig. 15A and column 14 as showing packets. However, Goodrum et al. do not call these illustrations "packets". These are disclosed as phases of a transaction, or contents of a memory queue. They are not a unit of data of finite size that is transmitted as a unit." The Examiner respectfully disagrees and finds this argument to be contradictive. The Applicant admits that these illustrations are phases of a transaction. By Applicant's own admission these bits shown in the table in column 14 are transmitted as a unit in a phase of a transaction. Further, the Applicant argues that these illustrations are not of a finite size, however, close examination of the table in column 14 shows the number of bits in each field, therefore, they are of finite size.

With respect to the argument: **C. <u>Whether Wolff et al. alone or in combination with Cepulis, Ardini, Jr. et al., Pizzica, Bershteyn et al., and/or Merrill et al. supports an obviousness rejection of claims 7-10, 14, 19, 23, 24, 35, and 36</u>**, on pages 7-8, the Applicant argues, "it is believed that Wolff et al. in combination with any or all of these reference cannot show or suggest the features of independent claims 1, 22, 35, and 36. For at least these reasons, claims 7-10, 14, 19, 23, 24, 35, and 36 are not made obvious by the applied references." The Examiner respectfully disagrees for at least the reasons above, which establish that Wolff et al. teach a packet bus and information packets.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

MM
August 18, 2004

Conferees
Donald Sparks
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